REMARKS

Claims 1-18 are pending in the present application. With entry of this Amendment, Applicants amend claims 1, 5, 7, 12, 14 and 16-18, cancel claim 3 and add new claims 19 and 20. Reexamination and reconsideration respectfully requested.

Applicants have amended independent claims 1, 12, 14, 16 and 18 to more clearly claim the present invention. New claims 19 and 20 depend from claims 12 and 14 respectively.

The Examiner rejected claims 1-8 and 11-18 under 35 U.S.C. §§ 102(b) or 103(a) as being either anticipated or obvious in view of Kuribayashi et al. (US 5539145).

Claim 1 is directed to a tone data processing device. The device comprises an input buffer, a processor and an output buffer. The input buffer receives waveform sample data from a storage device. The processor reads out the data from the input buffer and processes the data. The processed data is written into the output buffer. The processing performed by the processor includes converting the waveform sample rate of the read-out data to an inner sampling rate, performing arithmetic processing on the converted data, converting the data to a predetermined output sampling rate and writing the converted data to the output buffer. There are many advantages to having an inner sampling rate separate from the output sampling rate. For example, when employed by a tone generator LSI, it can reduce the processing loads on the LSI.

In contrast, Kuribayashi does not disclose such a device. Fig. 1 illustrates a record and reproduction control device RU that records a sound signal from a microphone. The sound signal is sampled and the digital waveform data is temporarily stored in a record buffer (RBUFA/B) and then stored in a hard disk HD (Col. 8, lines 14-21 and Fig. 2.). When data is to be reproduced, the data is transferred from the hard disk HD into a fetch buffer (XBUFA/B). After removing control data such as heading data, the data is transferred to a reproduction buffer (PBUFA/B) for subsequent read out by the tone generation circuit TG. This two stage buffer arrangement simplifies the read out by the TG (see Col. 9, line 47 to Col. 10, line 14). The TG reads out the data at a predetermined reproductive readout rate (Col. 9, lines 6-13).

The Examiner contends that the fetch buffer (XBUFA/B) reads on the input buffer of claim 1 because it receives data from the hard disk HD. The Examiner contends that the reproduction buffer (PBUFA/B) reads on the output buffer of claim 1. However, if one accepts the Examiner's contentions, none of the processing recited in claim 1 between the data read out from the input buffer to its writing in the output buffer is disclosed in Kuribayashi. All that occurs between the fetch buffer (XBUFA/B) and the reproduction buffer (PBUFA/B) is removing some control data to simplify tone reproduction by the TG (see Col. 9, line 47 to Col. 10, line 14). For example, there is no disclosure of a first process for reading out data from the inner buffer and converting the sampling rate of the data to an inner sampling rate.

The predetermined reproductive readout rate -- which the Examiner cites as disclosing a first reading process -- is applied to data readout from the reproduction buffer (PBUFA/B) (see Col. 9, lines 6-13). The reproduction buffer (PBUFA/B) is the output buffer in the Examiner's view. Kuribayashi does not disclose performing a first process of reading out data from the *input* buffer as recited in claim 1.

The Examiner's analysis of the recited second process further highlights the differences between the claimed invention and Kuribayashi. The second process performs arithmetic processing after the first process discussed above. Kuribayashi does not disclose any such processing. The Examiner cites the re-sampling circuit 21 which re-samples data to be stored in the record buffer (RBUFA/B). The data is then transferred to the hard disk HD. The cited process is, therefore, for writing data onto the hard disk HD. It is not processing performed on the data read out from the reproduction buffer (PBUFA/B). That is, Kuribayahsi fails to disclose the recited second process performed after the first process.

A similar conclusion can be reached with respect to the recited fourth process. The fourth process is writing the data into an output buffer after the third process of converting. The Examiner contends that the output buffer – reproduction buffer (PBUFA/B) – can receive information by the TG as indicated by the bi-directional arrow in Fig. 2. However, the bi-directional arrow merely indicates that the same clock pulses are input to the TG and PD. Fig. 2 clearly

illustrates that the flow of data is in one direction from the reproduction buffer (PBUFA/B) to the TG by using a uni-directional arrow immediately below the bi-directional arrow.

Accordingly, Applicants respectfully submit that claim 1 is not anticipated by Kuribayashi for at least the reasons discussed above. Claims 2, 4-8 and 11 which depend from claim 1 are not anticipated by or obvious in view of Kuribayashi for at least the reasons set forth above.

Independent claims 12 and 14 are not anticipated by Kuribayashi for at least the reasons discussed above. Claims 13 and 15 which depend from claim 12 and 14 respectively are not anticipated by or obvious in view of Kuribayashi for at least the reasons set forth above. Similarly, new claims 19 and 20 which depend from claims 12 and 14 respectively are in condition for allowance.

Claim 16 recites a first sampling conversion section which the Examiner contends as being met by the reading out of data from the reproduction buffer (PXBUFA/B) by the TG. Claim 16 further recites an arithmetic processing section performing processing on the data from the first conversion section which the Examiner contends as being met by the re-sampling circuit 21 sampling data to be given to the record buffer (RBUFA/B). The re-sampling circuit 21 relates to writing data onto hard disk HD and is not processing performed on the data read out from the reproduction buffer (PXBUFA/B). Accordingly, Applicants respectfully submit that claim 16 is not anticipated by Kuribayashi for at least the reasons discussed above. Claim 17 which depends from claim 16 is not anticipated by or obvious in view of Kuribayashi for at least the reasons set forth above.

Independent claim 18 is not anticipated by Kuribayashi for at least the reasons discussed above with respect to claim 16.

The Examiner rejected claim 9 under § 103(a) as being unpatentable over Kuribayashi in view of Hideo (US 5532424). Claim 10 was rejected under 103(a) as being unpatentable over Kuribayashi in view of Mitsuhashi (US 5127306). Neither Hideo nor Mitsuhashi make up for the

deficiencies of Kuribayashi. Accordingly, Applicants respectfully submit that claims 9 and 10 are patentable over the cited references.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If, for any reason, the Examiner finds the application other than in condition for allowance, Applicants request that the Examiner contact the undersigned attorney at the Los Angeles telephone number (213) 892-5630 to discuss any steps necessary to place the application in condition for allowance.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. 393032008800.

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Respectfully submitted,

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